APPLICATION

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TITLE: METHOD FOR FORMING FERROCAPACITORS AND FERAM DEVICES

APPLICANT: HAOREN ZHUANG, RAINER BRUCHHAUS, ULRICH EGGER, JINGYU LIAN AND NICOLAS NAGEL

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Method for forming ferrocapacitors and FeRAM devices

Field of the invention

The present invention relates to methods for forming ferrocapacitors of the kind used in FeRAM devices, and to methods for forming FeRAM devices themselves. The invention further relates to FeRAM devices including ferrocapacitors formed by the method.

Background of Invention

Many conventional FeRAM devices include a horizontal ferrocapacitor structure, in which a stack of layers is formed including top and bottom electrodes sandwiching a ferroelectric layer. An alternative "vertical capacitor" structure was suggested in US 6,300,652, the disclosure of which is incorporated herein by reference. A vertical capacitor includes a ferroelectric element sandwiched between electrodes to either side, all at substantially the same level in the FeRAM device.

The process steps of a conventional technique for forming a vertical capacitor structure are illustrated in Figs. 1 to 5. The vertical capacitors are typically to be formed over a substructure, which may for example be of the form shown in Fig. 1 in which various electronic components 1 are connected to conductive plugs 3 which extend upwards through a matrix 5 (e.g. of TEOS (tetraethylorthosilicate)). The upper ends of the plugs 3 terminate in TiN/Ir barrier elements 7, having a top surface flush with the surface of the matrix 5.

As shown in Fig. 2, an insulating layer 9 of Al_2O_3 is formed over the surface of the matrix 5, and a thicker layer of ferroelectric material 11 such as PZT ($PbZrTiO_3$) is formed over that.

As shown in Fig. 3, hardmask elements 13 are deposited over selected areas of the PZT layer 11, and the portions of the PZT 11 and Al_2O_3 9 which are not protected by the hardmask elements 13 are etched all the way through, forming openings 17. During this process Al_2O_3 fences 15 are often formed on the sides of the remaining PZT 11.

The openings 17 are then filled with conductive material 19 such as IrO_2, by depositing IrO_2 over the entire structure, as shown in Fig. 4, and chemical-mechanical planarization (CMP) polishing is performed to form a flat upper surface 21 which is partly the PZT 11 and partly the conductive material 19. Then, as shown in Fig. 5, an Al_2O_3 layer 23 is formed over the surface 19. The elements 19 of IrO_2 constitute electrodes, while the remaining PZT 11 forms the dielectric.

The vertical capacitor structure has great potential for reducing the cell size, especially if the etching taper angle of the remaining PZT 11 (i.e. the angle between the horizontal direction and the sides of the remaining PZT 11) is high. However, if the taper angle becomes close to 90°, the Al_2O_3 fences 15 are more likely to be formed. These fences 15 are difficult to remove (e.g. by a wet cleaning process), and dramatically reduce the Q_{sw} (i.e. the maximum charge which can be stored in the ferrocapacitor) because the insulating fences 15 reduce the effective area of the capacitor.

Another reason for wanting to achieve a high taper angle is because it increases the uniformity of the electric field in the ferrocapacitor. If the ferroelectric dielectric is thinner in its upper portion than in its lower portion then the electric field will be higher at the top of the ferrocapacitor than at the bottom. The lack of electric field uniformity can cause problems for drive voltage setting, and device operation abnormalities. For example, the upper part of the dielectric has to work at a higher electric field than necessary.

These problems would be reduced by increasing the taper angle to be very close to 90°, but as mentioned above this leads to thicker fences.

Summary of the Invention

The present invention aims to alleviate the above problem, at least partially, and in particular to provide a new and useful method for forming ferrocapacitors and FeRAM devices with improved properties.

In general terms, the present invention proposes that, rather than forming the electrodes in holes formed in the ferroelectric material, the electrodes should be formed over openings in the insulating layer before the ferroelectric material is deposited.

Thus, no step of etching the insulating layer is required after the interface between the electrodes and ferroelectric material is formed. Accordingly, the fence problem is removed.

Furthermore, the ferroelectric material is preferably formed as a layer on the sides of the electrodes, rather than to fill the gaps between the electrodes. This means that the thickness of the ferroelectric material is not determined by the geometry of the gaps between the electrodes. This means that the thickness of the capacitor dielectric can be controlled very accurately, which in turn makes it easier to ensure that the electric field across it is uniform. Furthermore, the thickness of the ferroelectric layer can be selected to match a desired drive voltage.

Preferably, the thickness of the ferroelectric layer is optimised (e.g. made more uniform on the sides of the electrode, or its thickness there reduced to a desired lower value) by a further etching step performed on it.

Optionally, the further etching step may remove portions of the ferroelectric material extending over the insulating layer.

The ferroelectric layer is preferably covered with a support material, so as to fill the gaps between the electrodes and form an even surface. The support material used to cover the ferroelectric material is preferably a conductive material (e.g. irdinium), which, according to what other components it is attached to, may act as a dummy electrode. Alternatively, the ferroelectric material may be at least partly covered by an insulating material (such as TEOS).

Optionally, a conductive material (e.g. platinum) may be deposited on the sides of the electrodes, between the electrodes and the ferroelectric material. Similarly, a layer of conductive material may be deposited on the side of the ferroelectric layer away from the electrode.

Specifically, one expression of the invention is a method for forming a ferrocapacitor comprising:

forming electrode elements over a substructure, the electrode elements being in electrical contact with electrically conductive elements extending into the substructure; and

depositing ferroelectric material between the electrode elements.

An alternative expression of the invention is an FeRAM device comprising electrode elements and ferroelectric elements, the electrode elements and ferroelectric elements being formed over a substructure, the electrodes being in electrical contact with electrically conductive elements extending into the substructure and the ferroelectric elements being arranged between the electrodes as layers formed on the lateral sides of the electrodes.

Brief Description of The Figures

Preferred features of the invention will now be described, for the sake of illustration only, with reference to the following figures in which:

Figs. 1 to 5 show the steps of a conventional method of forming vertical capacitors;

Figs. 6 to 10 show the steps of a method which is an embodiment of the invention; and

Figs. 11 to 13 show ferroelectric capacitors which are alternative embodiments of the invention.

Detailed Description of the embodiments

The method which is an embodiment of the invention will be explained with reference to Figs. 6 to 11. The vertical capacitor structure is formed in these figures over a substructure which is like the one shown in Fig. 1 except that the plugs 3 and barrier elements 7 have not been formed in the matrix 5. Elements shown in Figs. 1 to 5 which exactly correspond to elements in Figs. 6 to 11 are illustrated by the same reference numerals.

The first step of the method, as in the conventional method, is for an insulating layer 31 of Al_2O_3 to be formed over the substructure. Then an etching step is performed to produce openings in the matrix 5 and in insulating layer 31. The plugs 3 are then formed in these openings extending through the matrix 5 and Insulating layer 31, as shown in Fig. 6.

In a second step of the method, a layer 33 of conductive material (typically Iridium) is formed over the Al_2O_3 layer 31. Hardmask elements 34 are formed over conductiv layer 33, substantially above the plugs 3. These hardmask elements 34 are formed by a process in which a hardmask (TEOS) layer is

formed over the conductive layer 33, then a resist layer is formed over the TEOS layer, then a lithographic process is performed, then a harmmask open (oxide RIE) process, and finally an ashing process. Although only two such elements 34 are shown in Fig. 7, it is to be understood that the structure shown in Fig. 7 is only a portion of a complete structure which extends to either side of the part shown in Fig. 7, with a periodicity equal to the spacing of the hardmask elements 34. The hardmask elements 34 may, as viewed from above, be for example square or rectangular areas, or they may be a layer containing gaps of any of these shapes. Etching is carried out using the hardmask elements 34 to form openings 35 in the conductive layer 33. In the openings 35, the entire thickness of the conductive layer 33 is preferably completely removed (and optionally also an upper part of the layer 31). A thin layer 34 (typically in the range 1nm to 15nm) of IrO_2 is then formed over the sides of the remaining portions of the conductive layer 33 by RTO (rapid thermal oxidation) in an atmosphere containing oxygen, to give the structure shown in Fig. 7. The IrO_2 improves the crystallinity of the capacitor.

As shown in Fig. 8, a layer 39 of a ferroelectric material, e.g. PZT, is then formed over the structure of Fig. 7, including in particular portions 41 on the sides of the openings. The portions 41 will constitute the dielectric elements in the completed ferrocapacitor device, as explained below. The thickness of the layer 39 would typically be in the range 20nm to 200nm.

Further etching is then performed to reduce the thickness of the ferroelectric layer 39, while still leaving a film 42 of ferroelectric material extending across the insulating layer 31. Then, as shown in Fig. 9, the openings 35 are filled with support material 43, which may be a conductive material such as IrO_2.

Then, CMP polishing is performed to form a flat upp r surface 45 which is partly the PZT 39, partly the conductive material 33, partly the conductive

material 34, and partly the conductive support material 43. Then, an Al_2O_3 layer 47 is formed over the surface 45, to form the completed structure shown in Fig. 10. The conductive material 33 makes electrical contact with the plugs 3, thereby electrically connecting the electrodes 33 with desired electrical components of the substructure. The conductive material 43 acts as a dummy electrode.

Although only a single embodiment of the invention has been described in detail above, many variations of the method are possible within the scope of the invention as will be clear to a skilled reader. For example, three alternative structures which can be formed according to the invention are shown in Figs. 11 to 13 respectively. Elements of these figures which correspond exactly to elements of Figs. 6 to 10 are indicated by the same reference numerals.

Firstly, as shown in Fig. 11, the etching step which is performed between Figures 8 and 9 above may be continued to the point that the layer 42 extending over the insulating layer 31 is completely removed. This would have the advantage of making makes the electric field more uniform at the edges of the layers 41.

Secondly, layers of Pt may be included in the structure. For example, a Pt layer 49 can be provided between the conductive elements 33 and the portions 41 of the PZT layer 39, instead of or in addition to the layer 32. Another Pt layer could be between the PZT 39 and the conductive material 43, or may indeed replace the material 43 as shown in Fig. 12, which has a layer 49 of PZT in place of the layer 32 and in which the opening in the PZT is filled with Pt 51. The possibility of introducing Pt in this way may be useful for increasing the options available to the designer of the system, since the Pt can significantly modify the charact ristics of the capacitor.

Thirdly, the conductive material 43 (or the Pt which replaces it in Fig. 12), may contain an element 53 of non-conductive material (e.g. of TEOS), as shown in Fig. 13. Such a material does no harm, since only the part of the conductive material 43 near the PZT 39 plays any active role. The use of TEOS in this way is beneficial since it is a relatively low-cost material, the dummy electrode performance may be improved, and the ferroelectric device is provided with a more effective cover.

These three variations are combinable in any combination within the scope of the invention.